1. An apparatus for increased analog-to-digital conversion resolution, the apparatus comprising:

an analog-to-digital converter configured to convert an analog signal to digital values comprising a plurality of bits; and

an interpolator configured to detect a response time of at least one analog comparator within the analog-to-digital converter core and thereby provide at least one additional bit to the plurality of bits.

2. The apparatus of claim 1, wherein the interpolator is further configured to provide the at least one additional bit at a rate substantially equal to a conversion rate of the analog-to-digital converter.

3. The apparatus of claim 1, wherein the response time of the at least one analog comparator is detected by detecting a settling pattern of at least one bit of the plurality of bits.

4. The apparatus of claim 1, wherein the response time of the at least one analog comparator is detected by detecting a settling time of at least one bit of the plurality of bits.

5. A method for increased analog-to-digital conversion resolution, the method comprising:

converting an analog signal to digital values comprising a plurality of bits with an analog-to-digital converter;

detecting a response time of at least one analog comparator within the analog-to-digital converter core to provide at least one additional bit to the plurality of bits.

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6. The method of claim 5, wherein the at least one additional bit is provided at a rate substantially equal to a conversion rate of the analog-to-digital converter.

7. The method of claim 5, wherein the response time of the at least one analog comparator is detected by detecting a settling pattern of at least one bit of the plurality of bits.

8. The method of claim 5, wherein the response time of the at least one analog comparator is detected by detecting a settling time of at least one bit of the plurality of bits.

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